July 25, 2022

Active Track: Small signal, higher gain ~High-gain driver amplifier design competition~
Design and prototype a drive amplifier with highest gain!

Applicants: student
Preliminary review: Yes.
#Details of the preliminary review will be announced by e-mail after registration.

## 1. Target specifications

- Frequency: The amplifier should operate (have positive gain) from 3.6 GHz to 4.2 GHz.
- Gain: The amplifier should have more than 6 dB over the above frequency range.
- Board size: The amplifier should be fabricated on the board smaller than 60 mm x 30 mm x 30 mm. Protrusions such as connectors are excluded. (See figure 2)

## 2. Evaluation rules

The attendee with highest total score is a winner of this contest. The total score is calculated in the following three below evaluation items: (a)Gain, (b)Gain flatness, and (c)Size. The points are given in response to the rank in each item. The point distribution is determined in Table 1.

If the total score is tied, the attendee with the highest (a)gain will be given priority.

(a) **Gain**:

"Gain" is evaluated the minimum gain from 3.6 GHz to 4.2 GHz. The higher this evaluation value, the better. Refer to figure 1 for the evaluation value.

The amplifier must meet "1. Target specifications" and "3. Design conditions." Otherwise, the point of this item is zero.

(b) **Gain flatness**:

"Gain flatness" is evaluated the deviation between the maximum gain and the minimum gain from 3.6 GHz to 4.2 GHz. The smaller this evaluation value, the better. Refer to figure 1 for the evaluation value.

The amplifier must meet "1. Target specifications" and "3. Design conditions." Otherwise, the point of this item is zero.

(c) **Size**:

"Size" is evaluated the following the board area: X (≦ 60 mm) x Y (≦ 30 mm) $mm^2$. The smaller this evaluation value, the better. Refer to figure 2 for the evaluation value.

The amplifier must meet "1. Target specifications" and "3. Design conditions." Otherwise, the point of this item is zero.

Table 1. Rank and score

| Evaluations / Rank | (a) Gain | (b) Gain flatness | (c) Board size |
|---|---|---|---|
| 1st | 20 | 20 | 10 |
| 2nd | 18 | 18 | 9 |
| 3rd | 16 | 16 | 8 |
| 4th | 14 | 14 | 7 |
| 5th | 12 | 12 | 6 |
| 6th | 10 | 10 | 5 |
| 7th | 8 | 8 | 4 |
| 8th | 6 | 6 | 3 |
| 9th | 4 | 4 | 2 |
| 10th~ | 2 | 2 | 1 |

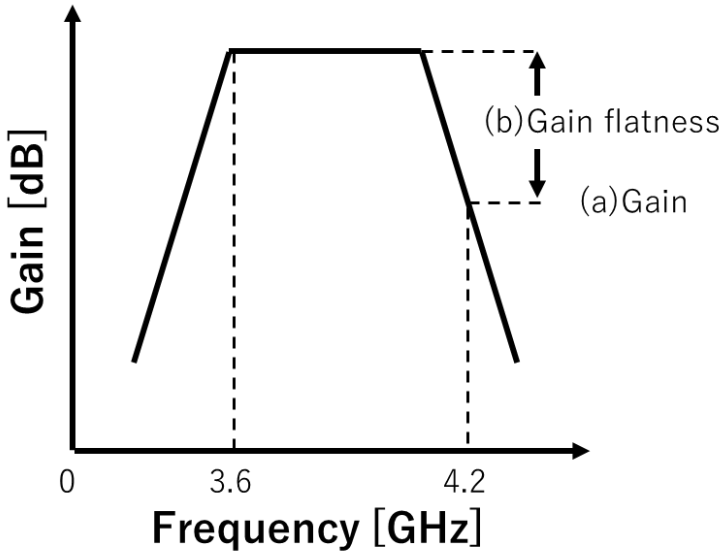


Figure1. Evaluation value of Gain and Gain flatness.

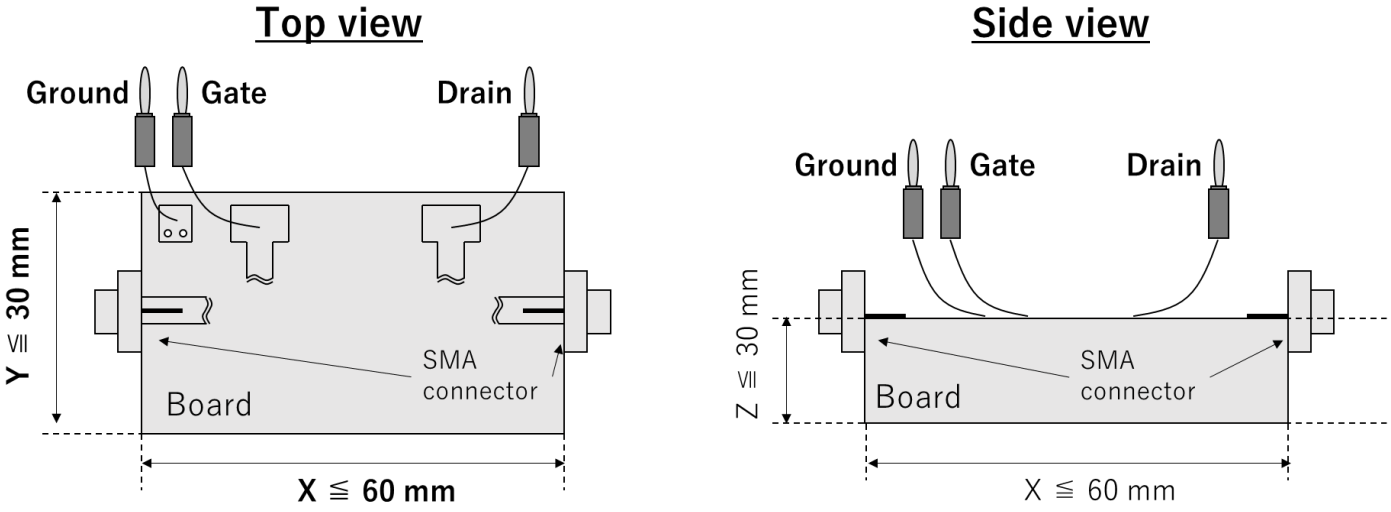


Figure 2. Evaluation value of Board size.

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## 3. Design conditions

(a) The attendee must use the following transistor: CE3514M4-C2 made by California Eastern Laboratories (CEL). The attendee must need to obtain their own transistors. Refer of the following site.

i DigiKey:
https://www.digikey.jp/ja/products/detail/cel/CE3514M4-C2/6165461

ii Mouser:
https://www.mouser.jp/ProductDetail/CEL/CE3514M4-C2?qs=tucQmhgEO3r12g7Kl95eJw%3D%3D

iii Chip 1 stop:
https://www.chip1stop.com/view/dispDetail/DispDetail?mpn=CE3514M4-C2&partId=CEL1-0005074

(b) The amplifier must be single stage.

(c) The amplifier must have the bias circuits. The bias connections should be male banana plugs ($\phi$4mm banana plugs).

(d) The amplifier must have DC cut capacitors or couplers at input and output port.

(e) The voltage and the current of the drain bias must be less than 2 V and less than 15 mA, respectively.

(f) The maximum input power level of the amplifier must be less than -20 dBm by the CW test.

(g) The connectors of input and output ports of the amplifier must be female SMA connectors which are ISO metric screw threads. Don't use inch size connectors.

(h) The reflection gain of input and output of the amplifier should be less than 0 dB from 100 MHz to 15 GHz when applying the gate and drain voltages.

(i) The stability factor of the amplifier should be more than K=1 from 100 MHz to 15 GHz when applying the gate and drain voltages.

(j) The board shape of the amplifier must be square or rectangular.

(k) The attendee can be shorted the GND terminal of the power supply to RF GND of SMA connectors.

## 4. Experimental Environments on Site

The following equipment will be prepared by the SDC committee for the evaluation at the competition:

(a) A vector network analyzer

(b) A power supply for drain bias through female banana plug.

(c) A power supply for gate bias through female banana plug.

The attendee must complete the measurement within the specified time limit.

## 5. Notes

If you cannot participate onsite, you can send your work to SDC committee. Postal address will later be notified. SDC committee will evaluate your work on your behalf. SDC committee will discard your work, not returning to you.